FIG. 1

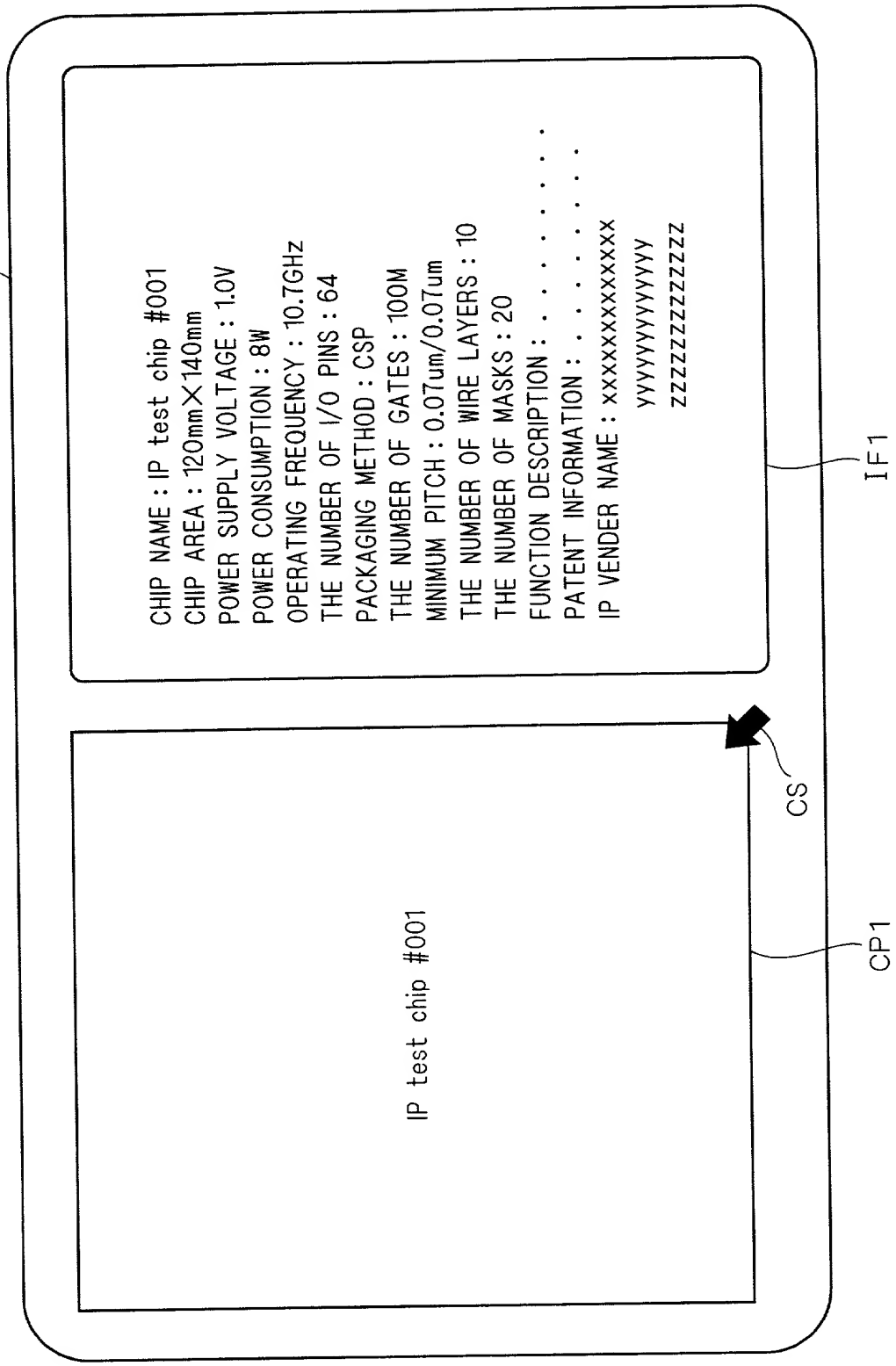

P01
CHIP NAME : IP test chip #001
CHIP AREA : 120mm×140mm
POWER SUPPLY VOLTAGE : 1.0V
POWER CONSUMPTION : 8W
OPERATING FREQUENCY : 10.7GHz
THE NUMBER OF I/O PINS : 64
PACKAGING METHOD : CSP
THE NUMBER OF GATES : 100M
MINIMUM PITCH : 0.07um/0.07um
THE NUMBER OF WIRE LAYERS : 10
THE NUMBER OF MASKS : 20
FUNCTION DESCRIPTION : . . . . . .
PATENT INFORMATION : . . . . . .
IP VENDER NAME : xxxxxxxxxxxx
yyyyyyyyyyyy
zzzzzzzzzzzz
IF1
IP test chip #001
CS
CP1

FIG. 2

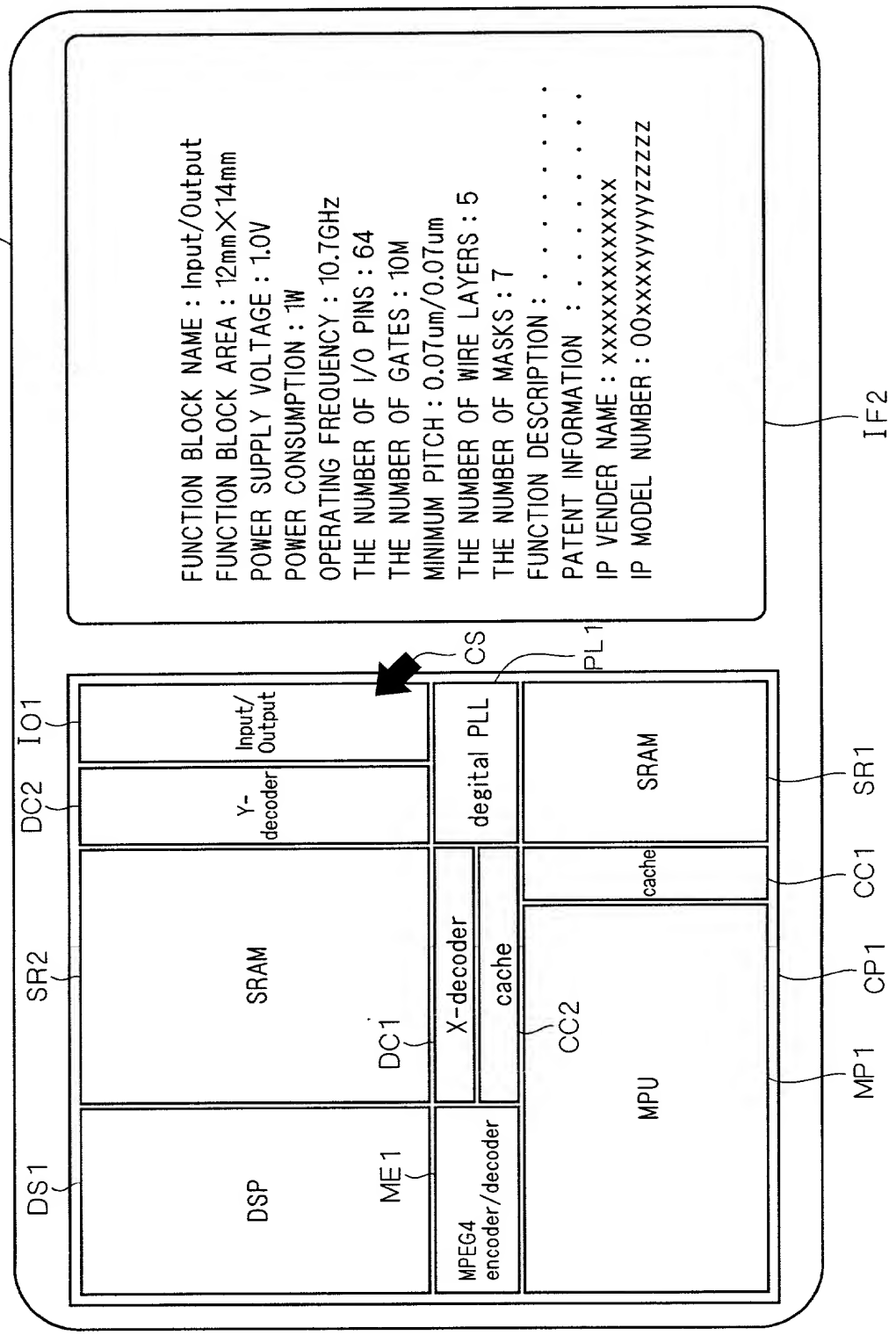

P02
FUNCTION BLOCK NAME : Input/Output
FUNCTION BLOCK AREA : 12mm×14mm
POWER SUPPLY VOLTAGE : 1.0V
POWER CONSUMPTION : 1W
OPERATING FREQUENCY : 10.7GHz
THE NUMBER OF I/O PINS : 64
THE NUMBER OF GATES : 10M
MINIMUM PITCH : 0.07um/0.07um
THE NUMBER OF WIRE LAYERS : 5
THE NUMBER OF MASKS : 7
FUNCTION DESCRIPTION : . . . . . .
PATENT INFORMATION : . . . . . .
IP VENDER NAME : xxxxxxxxxxxx
IP MODEL NUMBER : 00xxxxyyyyyzzzzz
IF2
IO1
DC2
Input/ Output
Y- decoder
CS
PL1
degital PLL
SR1
SRAM
SR2
SRAM
DC1
X-decoder
cache
CC1
cache
CC2
DS1
DSP
ME1
MPEG4 encoder/decoder
MPU
MP1
CP1

FIG. 3

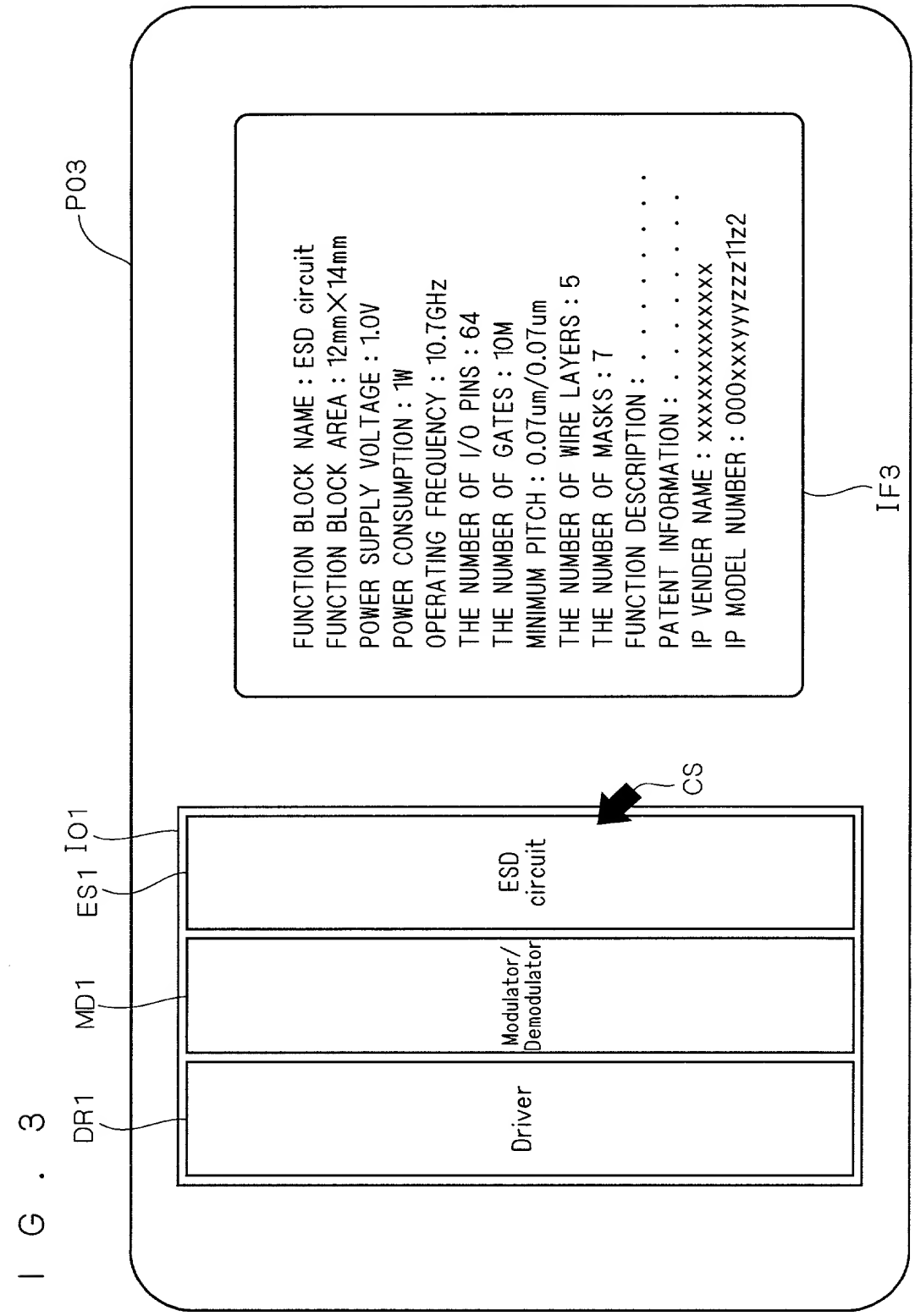

P03
FUNCTION BLOCK NAME : ESD circuit
FUNCTION BLOCK AREA : 12mm×14mm
POWER SUPPLY VOLTAGE : 1.0V
POWER CONSUMPTION : 1W
OPERATING FREQUENCY : 10.7GHz
THE NUMBER OF I/O PINS : 64
THE NUMBER OF GATES : 10M
MINIMUM PITCH : 0.07um/0.07um
THE NUMBER OF WIRE LAYERS : 5
THE NUMBER OF MASKS : 7
FUNCTION DESCRIPTION : . . . . . .
PATENT INFORMATION : . . . . . .
IP VENDER NAME : xxxxxxxxxxxx
IP MODEL NUMBER : 000xxxyyyzzz11z2
IF3
CS
IO1
ES1
ESD circuit
MD1
Modulator/ Demodulator
DR1
Driver

FIG. 4

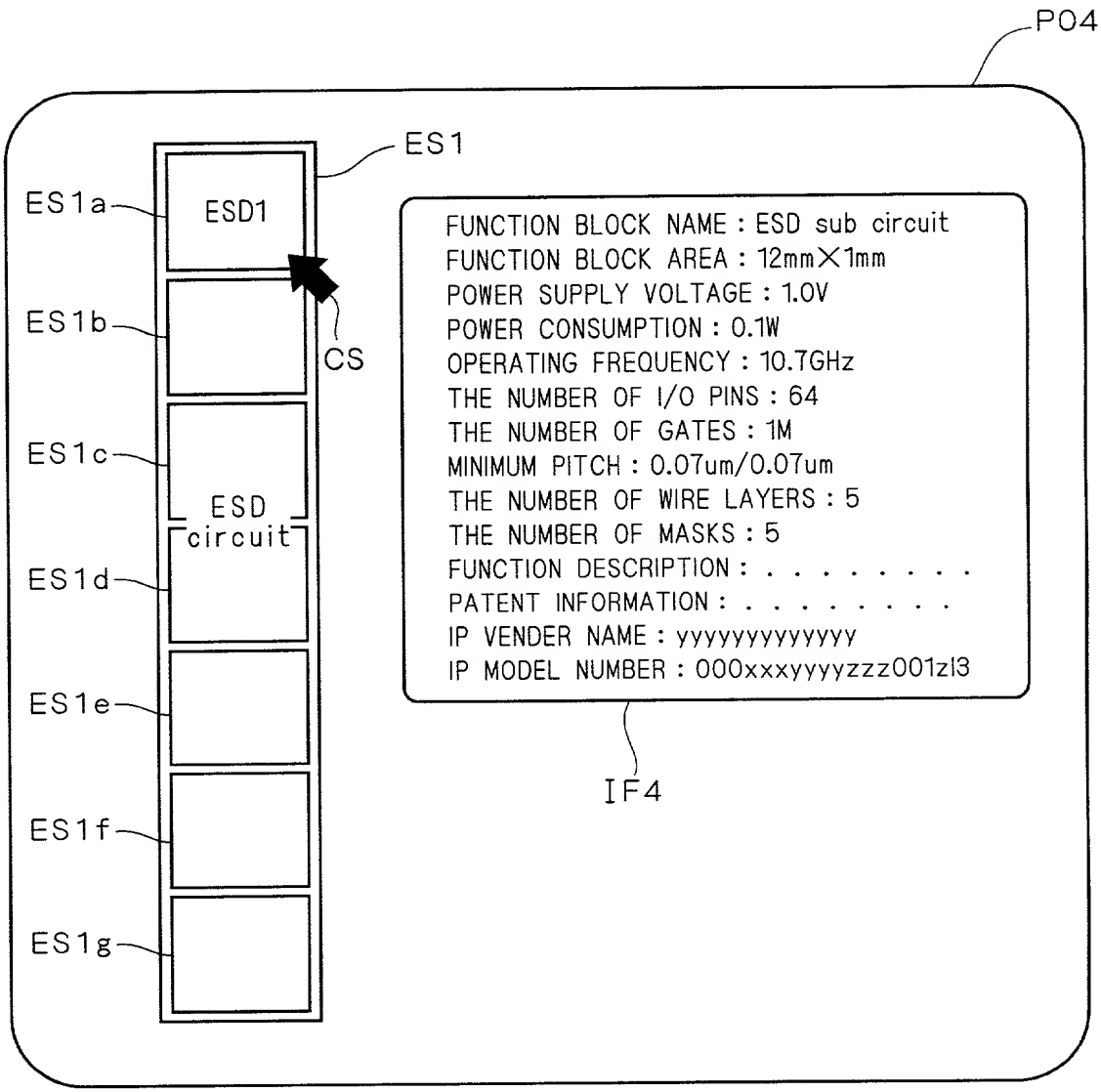

P04
ES1
ES1a
ESD1
ES1b
CS
ES1c
ESD
circuit
ES1d
ES1e
ES1f
ES1g
FUNCTION BLOCK NAME : ESD sub circuit
FUNCTION BLOCK AREA : 12mm×1mm
POWER SUPPLY VOLTAGE : 1.0V
POWER CONSUMPTION : 0.1W
OPERATING FREQUENCY : 10.7GHz
THE NUMBER OF I/O PINS : 64
THE NUMBER OF GATES : 1M
MINIMUM PITCH : 0.07um/0.07um
THE NUMBER OF WIRE LAYERS : 5
THE NUMBER OF MASKS : 5
FUNCTION DESCRIPTION : . . . . . .
PATENT INFORMATION : . . . . . .
IP VENDER NAME : yyyyyyyyyyyyy
IP MODEL NUMBER : 000xxxyyyyzzz001zl3
IF4

FIG. 5

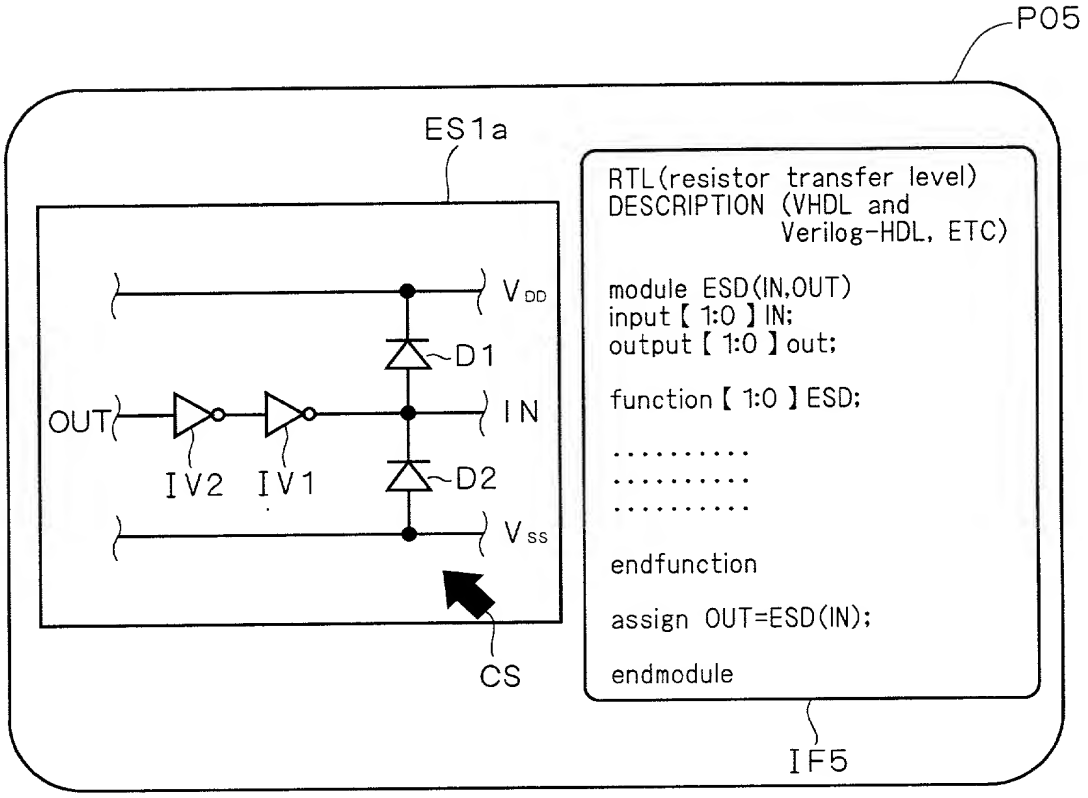
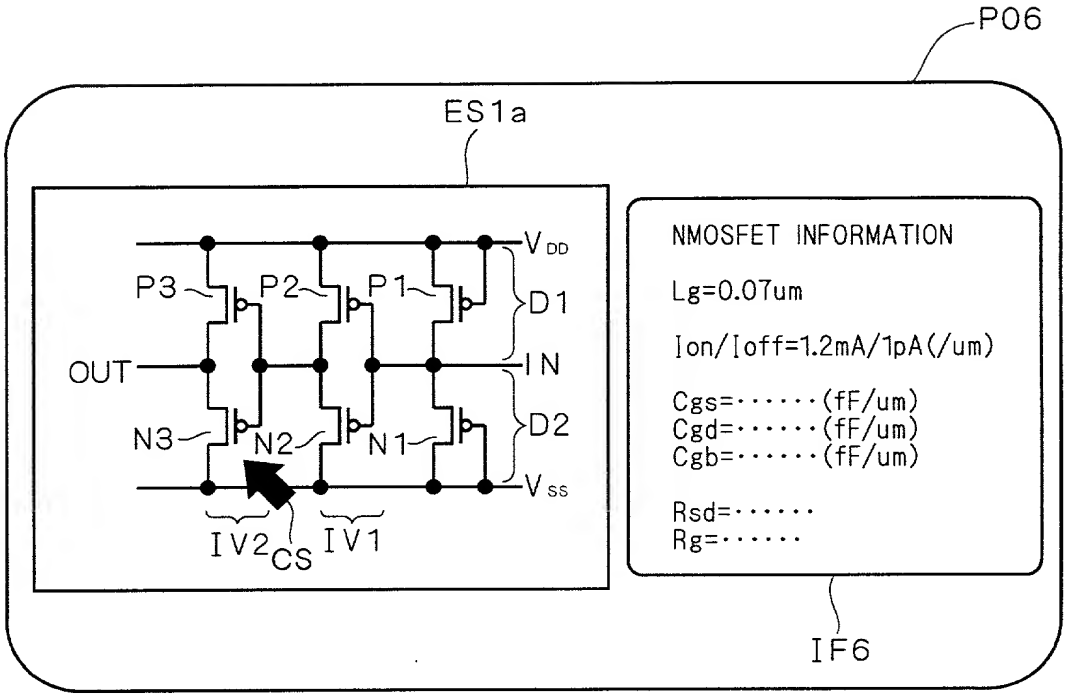

P05
ES1a
VDD
D1
OUT
IN
IV2
IV1
D2
Vss
CS
RTL(resistor transfer level)
DESCRIPTION (VHDL and
Verilog-HDL, ETC)
module ESD(IN,OUT)
input [1:0] IN;
output [1:0] out;
function [1:0] ESD;
.....
.....
.....
endfunction
assign OUT=ESD(IN);
endmodule
IF5

FIG. 6


P06
ES1a
VDD
P3
P2
P1
D1
OUT
IN
N3
N2
N1
D2
VSS
IV2
CS
IV1
NMOSFET INFORMATION
Lg=0.07um
Ion/Ioff=1.2mA/1pA(/um)
Cgs=·····(fF/um)
Cgd=·····(fF/um)
Cgb=·····(fF/um)
Rsd=·····
Rg=·····
IF6

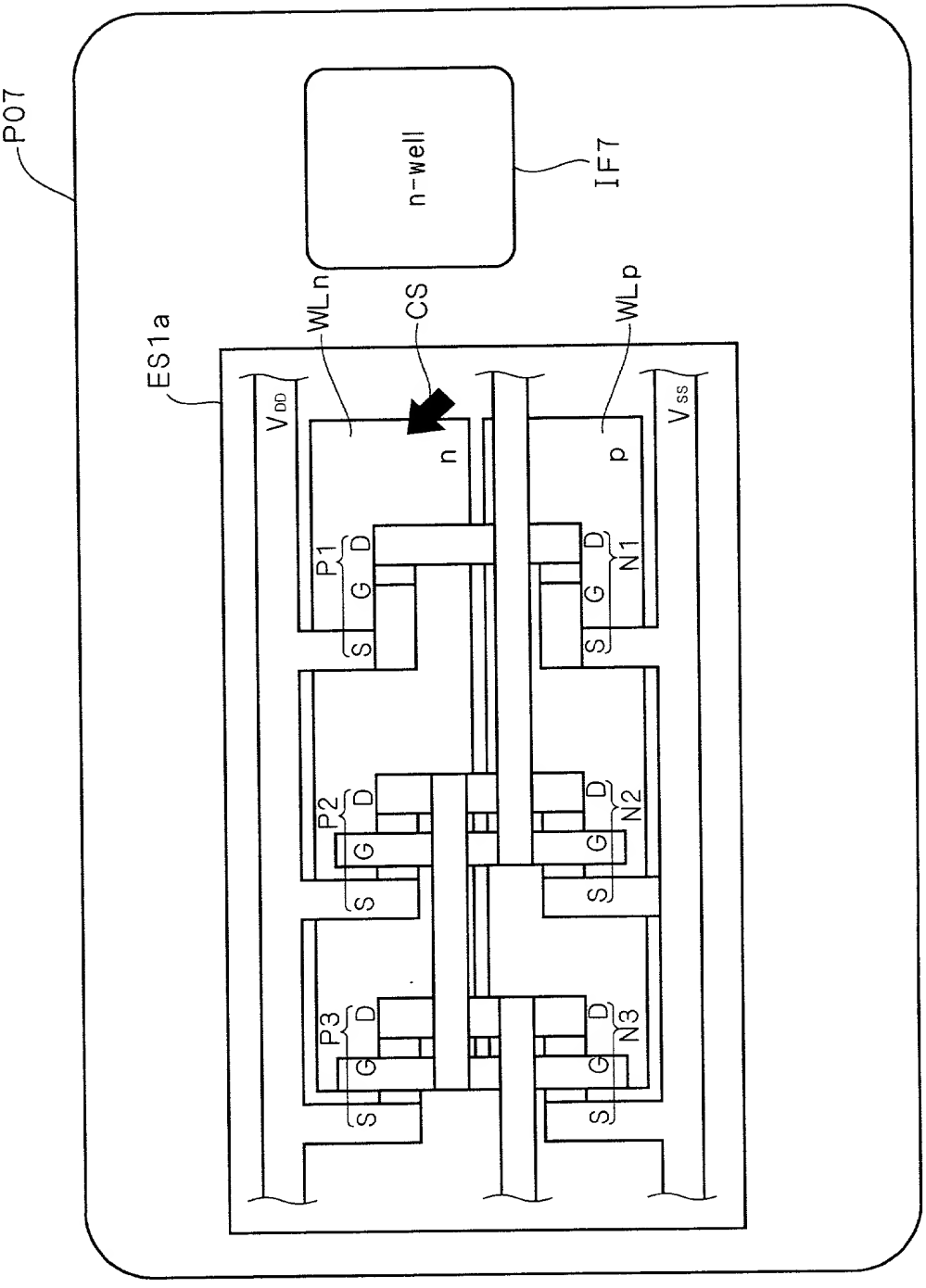


FIG. 7

FIG. 8

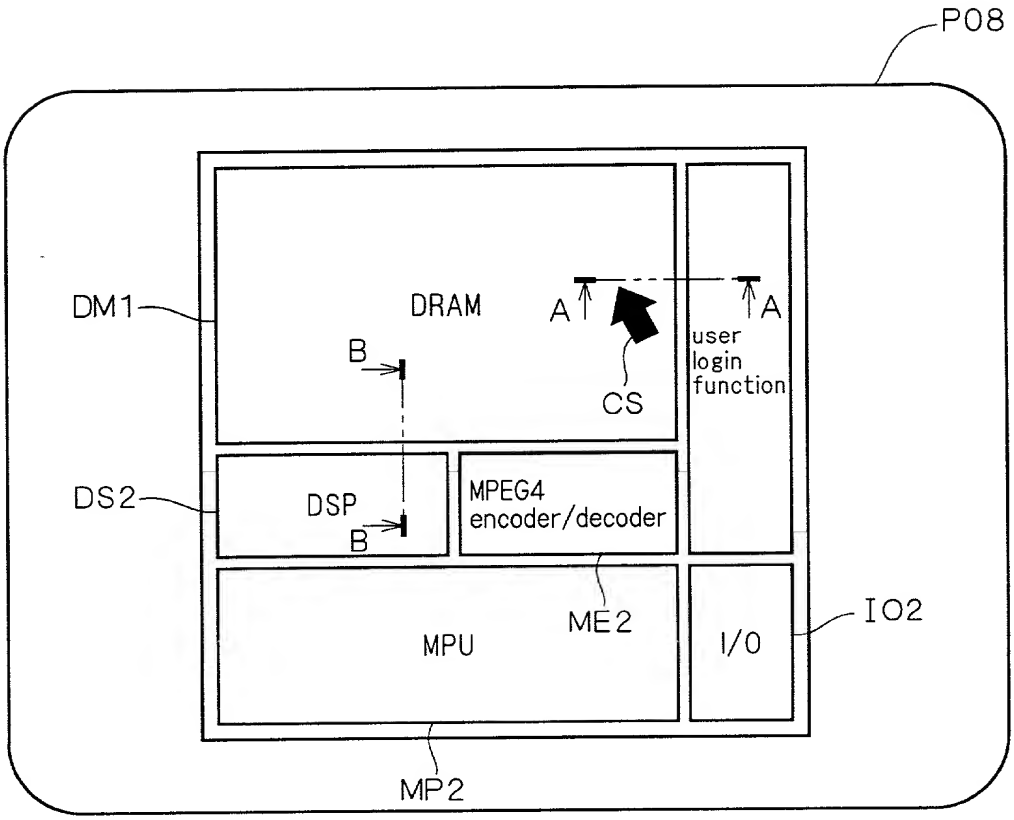

P08
DM1
DRAM
A
A
B
user
login
function
CS
DS2
DSP
B
MPEG4
encoder/decoder
ME2
IO2
MPU
I/O
MP2

FIG. 9

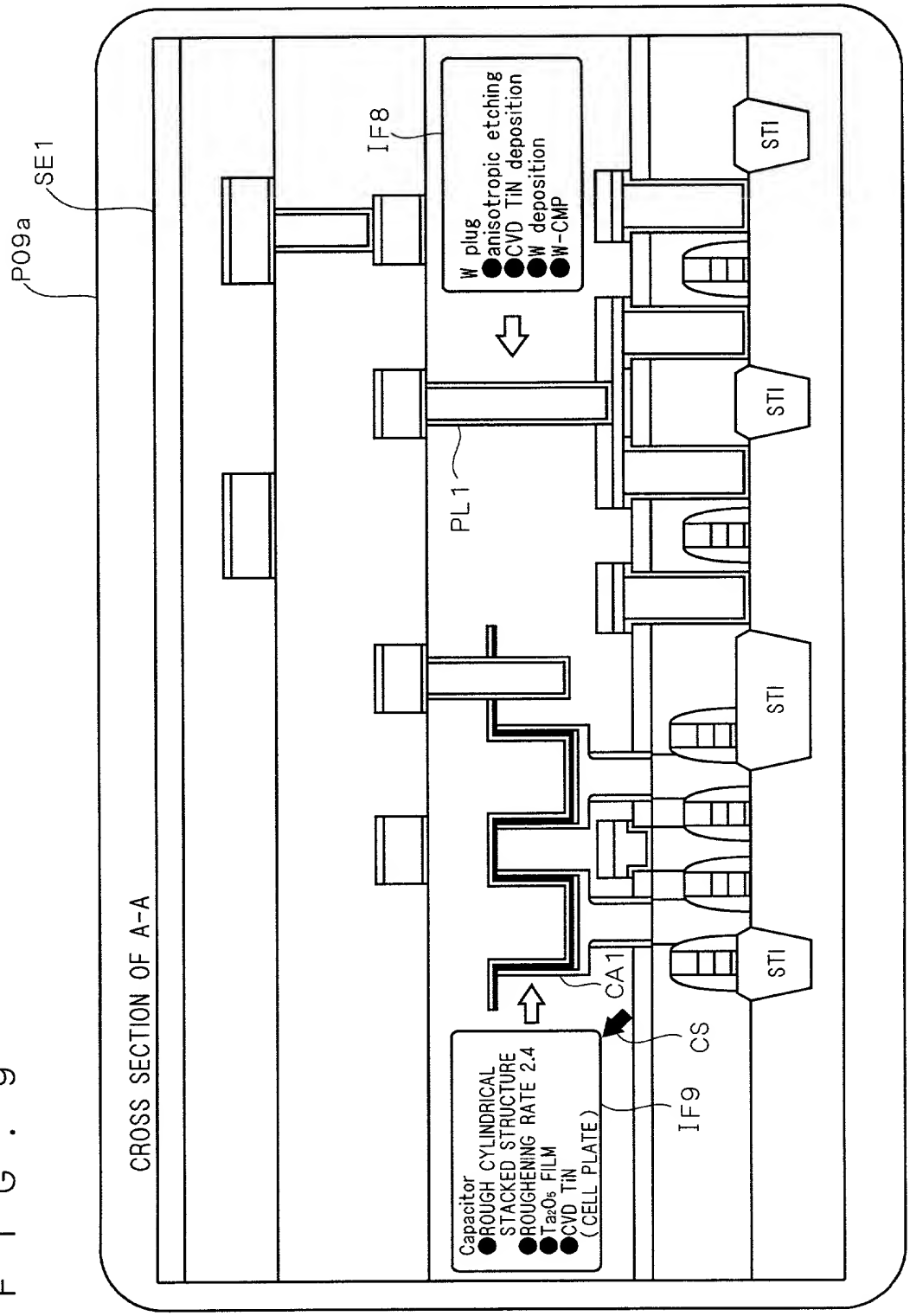

CROSS SECTION OF A-A
P09a
SE1
IF8
W plug
anisotropic etching
CVD TiN deposition
W deposition
W-CMP
PL1
STI
STI
STI
STI
CA1
CS
IF9
Capacitor
ROUGH CYLINDRICAL STACKED STRUCTURE
ROUGHENING RATE 2.4
Ta_2O_5 FILM
CVD TiN
(CELL PLATE)

FIG. 10

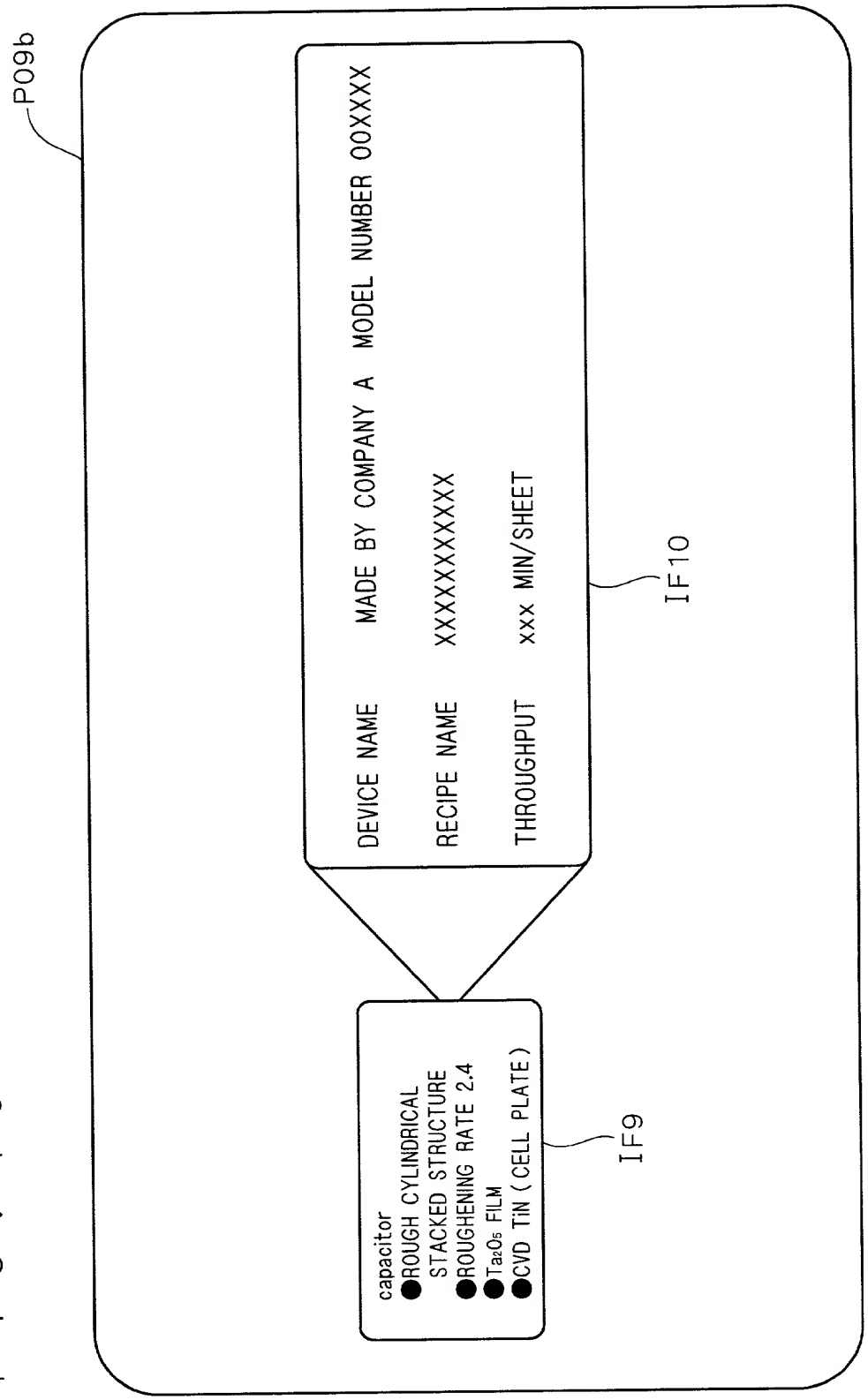

P09b
DEVICE NAME
MADE BY COMPANY A MODEL NUMBER OOXXXX
RECIPE NAME
XXXXXXXXXX
THROUGHPUT
xxx MIN/SHEET
IF10
capacitor
●ROUGH CYLINDRICAL STACKED STRUCTURE
●ROUGHENING RATE 2.4
●Ta2O5 FILM
●CVD TiN (CELL PLATE)
IF9

FIG. 11

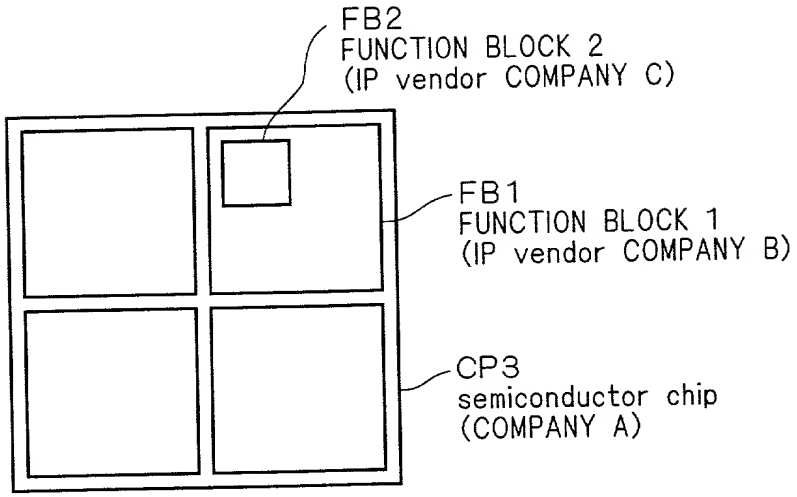

FB2
FUNCTION BLOCK 2
(IP vendor COMPANY C)
FB1
FUNCTION BLOCK 1
(IP vendor COMPANY B)
CP3
semiconductor chip
(COMPANY A)

FIG. 12

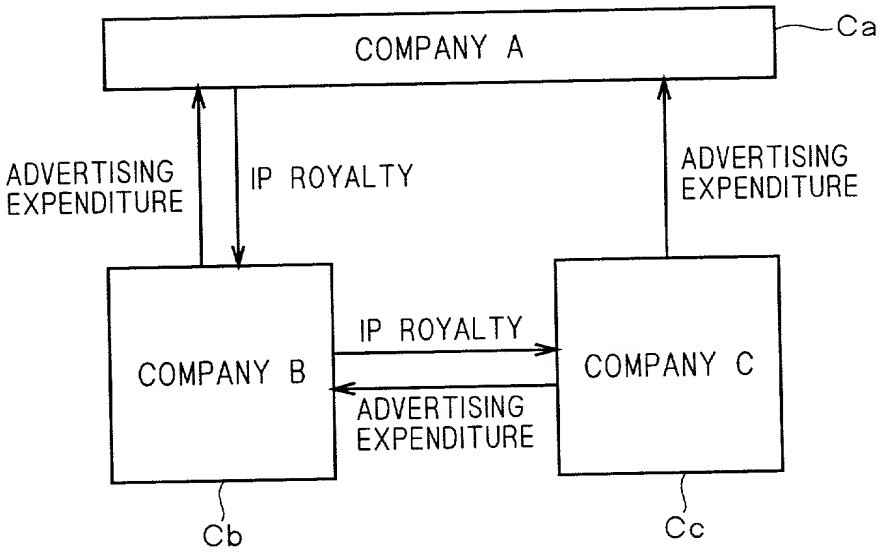

COMPANY A
Ca
ADVERTISING EXPENDITURE
IP ROYALTY
ADVERTISING EXPENDITURE
COMPANY B
IP ROYALTY
ADVERTISING EXPENDITURE
COMPANY C
Cb
Cc

FIG. 13

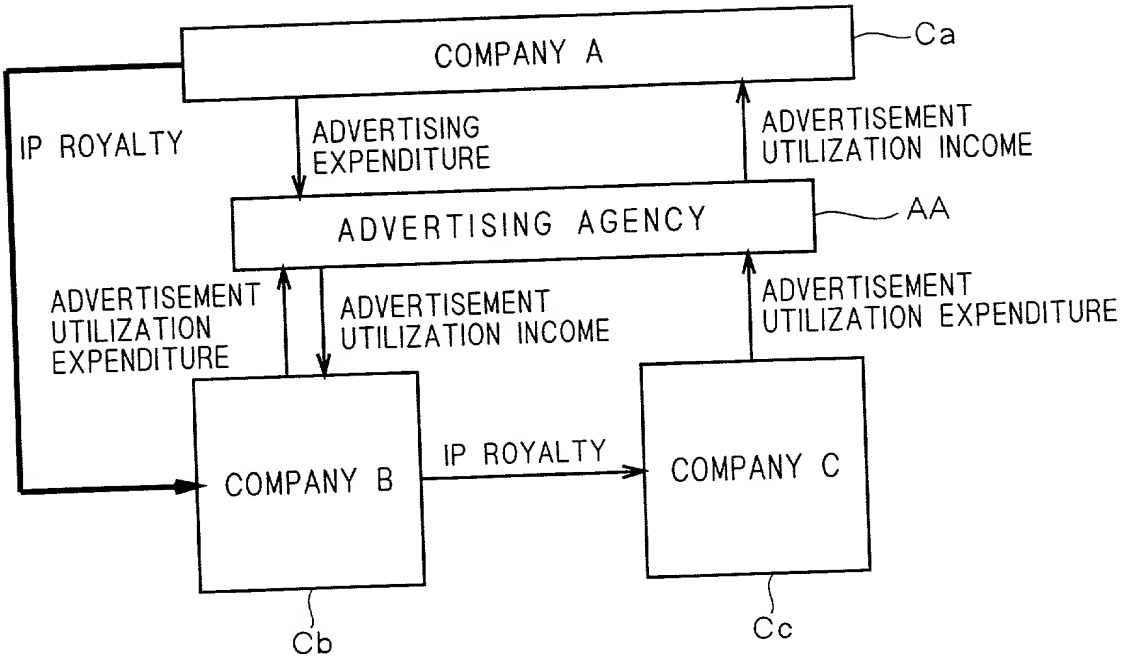

COMPANY A
Ca
IP ROYALTY
ADVERTISING EXPENDITURE
ADVERTISEMENT UTILIZATION INCOME
ADVERTISING AGENCY
AA
ADVERTISEMENT UTILIZATION EXPENDITURE
ADVERTISEMENT UTILIZATION INCOME
ADVERTISEMENT UTILIZATION EXPENDITURE
COMPANY B
IP ROYALTY
COMPANY C
Cb
Cc

FIG. 14

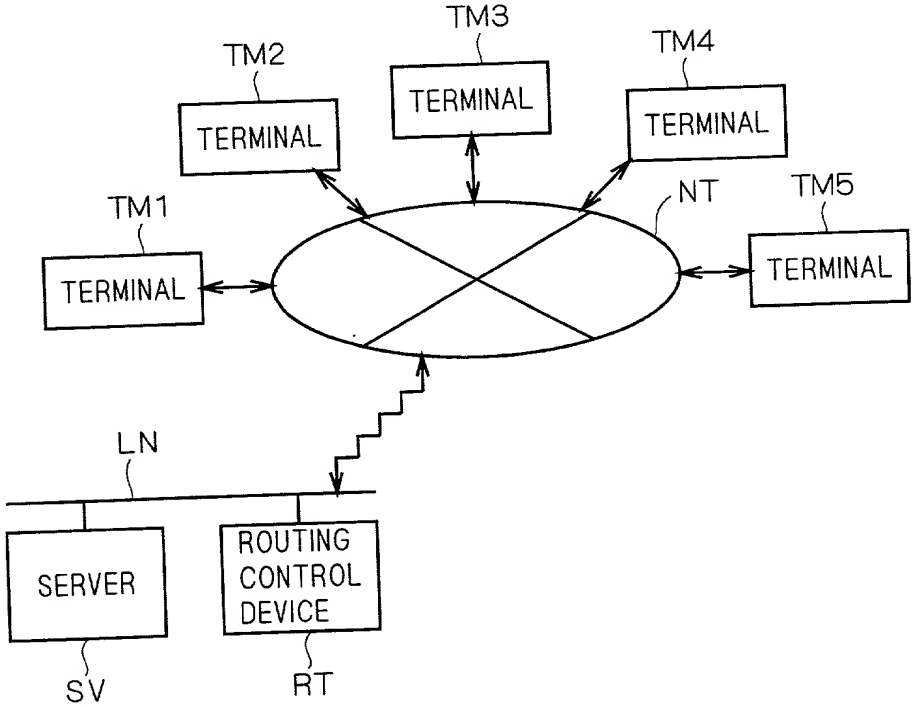

TM1
TM2
TM3
TM4
TM5
TERMINAL
TERMINAL
TERMINAL
TERMINAL
TERMINAL
NT
LN
SERVER
ROUTING CONTROL DEVICE
SV
RT

FIG. 15

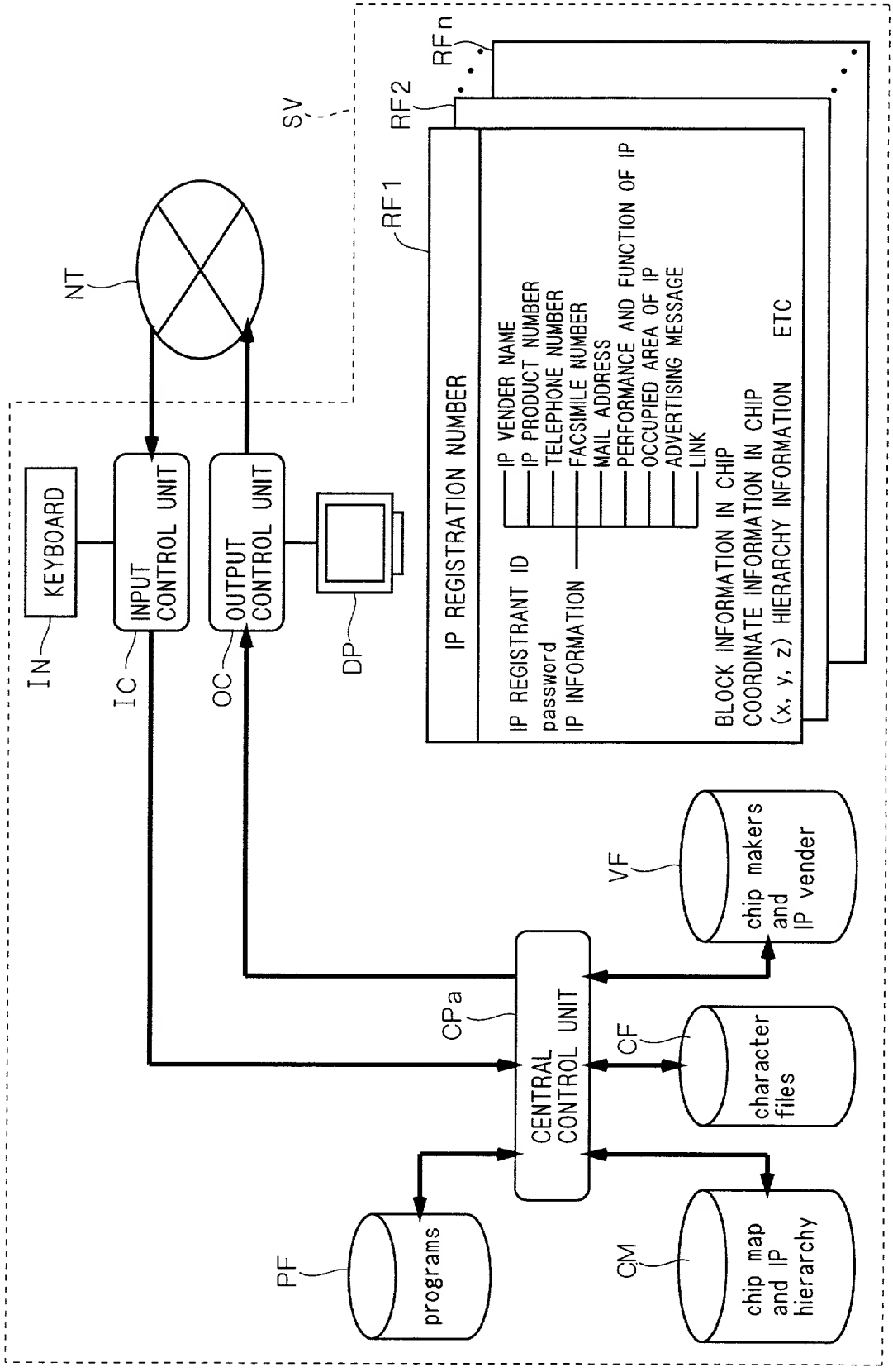

SV
NT
KEYBOARD
IN
INPUT CONTROL UNIT
IC
OUTPUT CONTROL UNIT
OC
DP
CPa
CENTRAL CONTROL UNIT
PF
programs
CF
character files
CM
chip map and IP hierarchy
VF
chip makers and IP vender
RF1
RF2
RFn
IP REGISTRATION NUMBER
IP REGISTRANT ID
password
IP INFORMATION
IP VENDER NAME
IP PRODUCT NUMBER
TELEPHONE NUMBER
FACSIMILE NUMBER
MAIL ADDRESS
PERFORMANCE AND FUNCTION OF IP
OCCUPIED AREA OF IP
ADVERTISING MESSAGE
LINK
BLOCK INFORMATION IN CHIP
COORDINATE INFORMATION IN CHIP
(x, y, z) HIERARCHY INFORMATION
ETC

FIG. 16

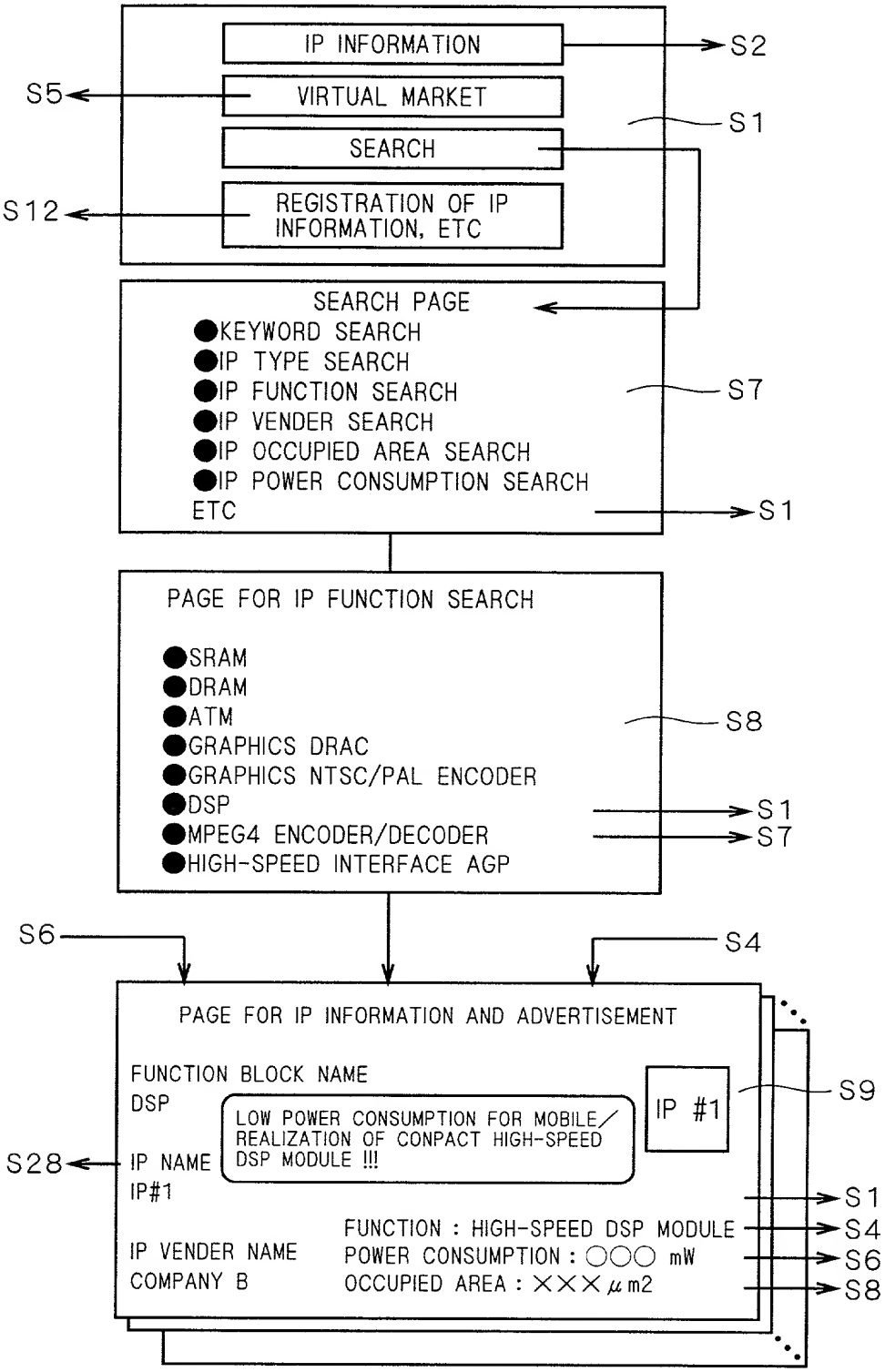

IP INFORMATION
S2
S5
VIRTUAL MARKET
SEARCH
S1
S12
REGISTRATION OF IP INFORMATION, ETC
SEARCH PAGE
●KEYWORD SEARCH
●IP TYPE SEARCH
●IP FUNCTION SEARCH
●IP VENDER SEARCH
●IP OCCUPIED AREA SEARCH
●IP POWER CONSUMPTION SEARCH
ETC
S7
S1
PAGE FOR IP FUNCTION SEARCH
●SRAM
●DRAM
●ATM
●GRAPHICS DRAC
●GRAPHICS NTSC/PAL ENCODER
●DSP
●MPEG4 ENCODER/DECODER
●HIGH-SPEED INTERFACE AGP
S8
S1
S7
S6
S4
PAGE FOR IP INFORMATION AND ADVERTISEMENT
FUNCTION BLOCK NAME
DSP
LOW POWER CONSUMPTION FOR MOBILE/ REALIZATION OF CONPACT HIGH-SPEED DSP MODULE !!!
IP #1
S9
S28
IP NAME
IP#1
S1
FUNCTION : HIGH-SPEED DSP MODULE
S4
IP VENDER NAME
COMPANY B
POWER CONSUMPTION : ○○○ mW
S6
OCCUPIED AREA : ××× μm2
S8

FIG. 17

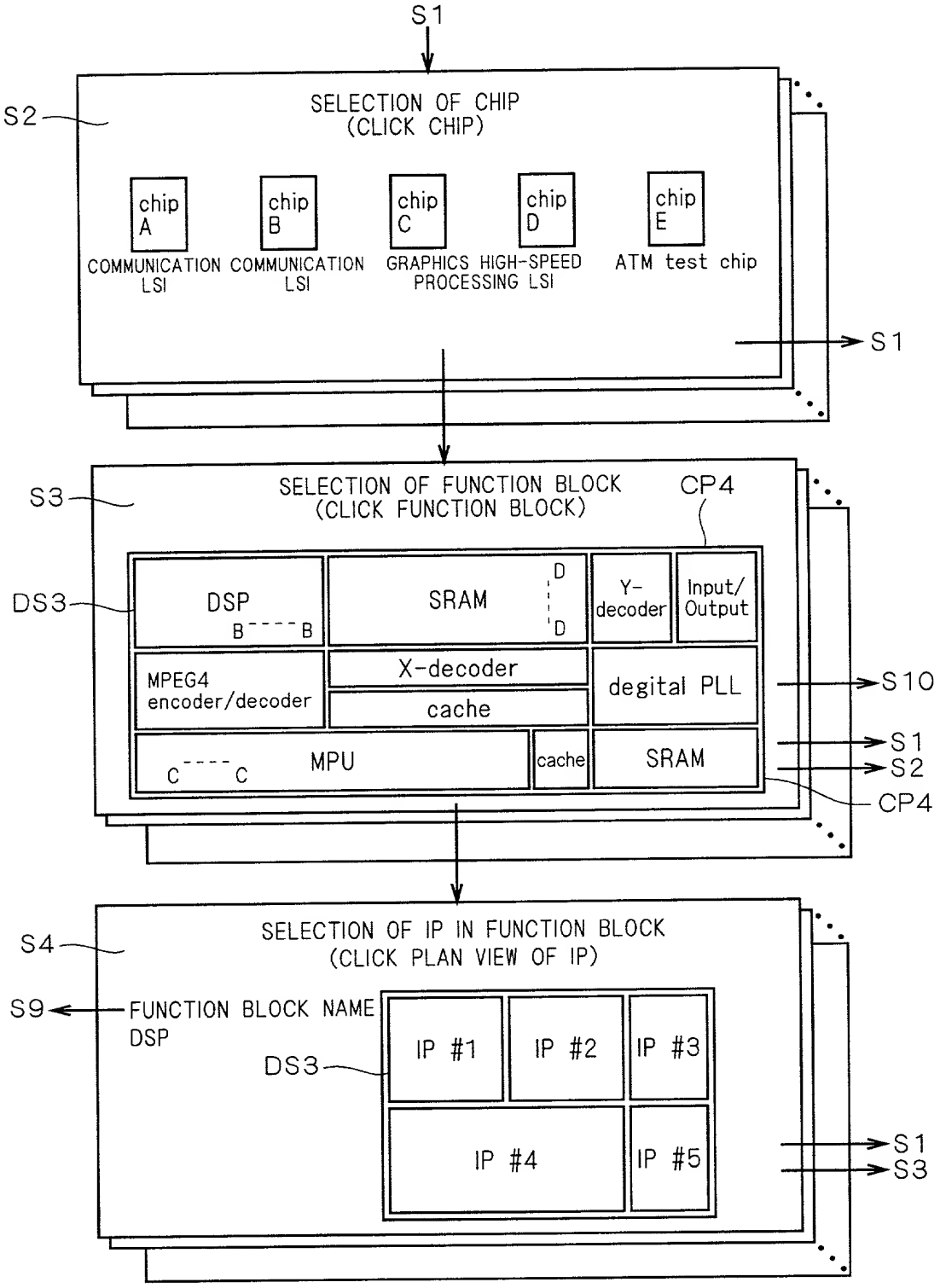

S1
S2
SELECTION OF CHIP
(CLICK CHIP)
chip A
chip B
chip C
chip D
chip E
COMMUNICATION LSI
COMMUNICATION LSI
GRAPHICS PROCESSING LSI
HIGH-SPEED
ATM test chip
S1
S3
SELECTION OF FUNCTION BLOCK
(CLICK FUNCTION BLOCK)
CP4
DS3
DSP
B B
SRAM
D D
Y-decoder
Input/Output
MPEG4 encoder/decoder
X-decoder
cache
degital PLL
S10
C C
MPU
cache
SRAM
S1
S2
CP4
S4
SELECTION OF IP IN FUNCTION BLOCK
(CLICK PLAN VIEW OF IP)
S9
FUNCTION BLOCK NAME
DSP
DS3
IP #1
IP #2
IP #3
IP #4
IP #5
S1
S3

FIG. 18

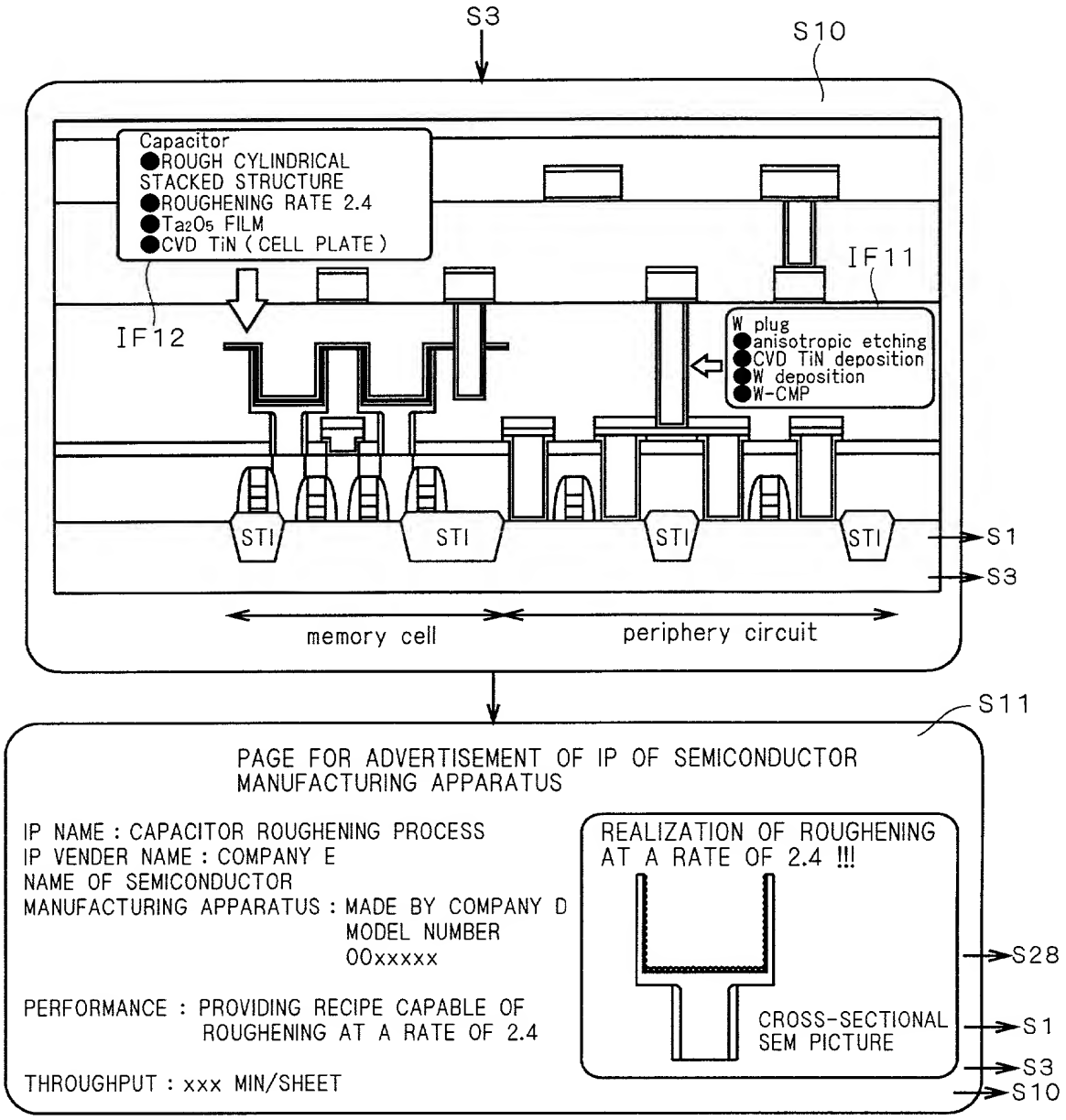

S3
S10
Capacitor
●ROUGH CYLINDRICAL STACKED STRUCTURE
●ROUGHENING RATE 2.4
●Ta2O5 FILM
●CVD TiN (CELL PLATE)
IF12
IF11
W plug
●anisotropic etching
●CVD TiN deposition
●W deposition
●W-CMP
STI
STI
STI
STI
S1
S3
memory cell
periphery circuit
S11
PAGE FOR ADVERTISEMENT OF IP OF SEMICONDUCTOR MANUFACTURING APPARATUS
IP NAME : CAPACITOR ROUGHENING PROCESS
IP VENDER NAME : COMPANY E
NAME OF SEMICONDUCTOR MANUFACTURING APPARATUS : MADE BY COMPANY D
MODEL NUMBER
00xxxxx
PERFORMANCE : PROVIDING RECIPE CAPABLE OF ROUGHENING AT A RATE OF 2.4
THROUGHPUT : xxx MIN/SHEET
REALIZATION OF ROUGHENING AT A RATE OF 2.4 !!!
CROSS-SECTIONAL SEM PICTURE
S28
S1
S3
S10

FIG. 19

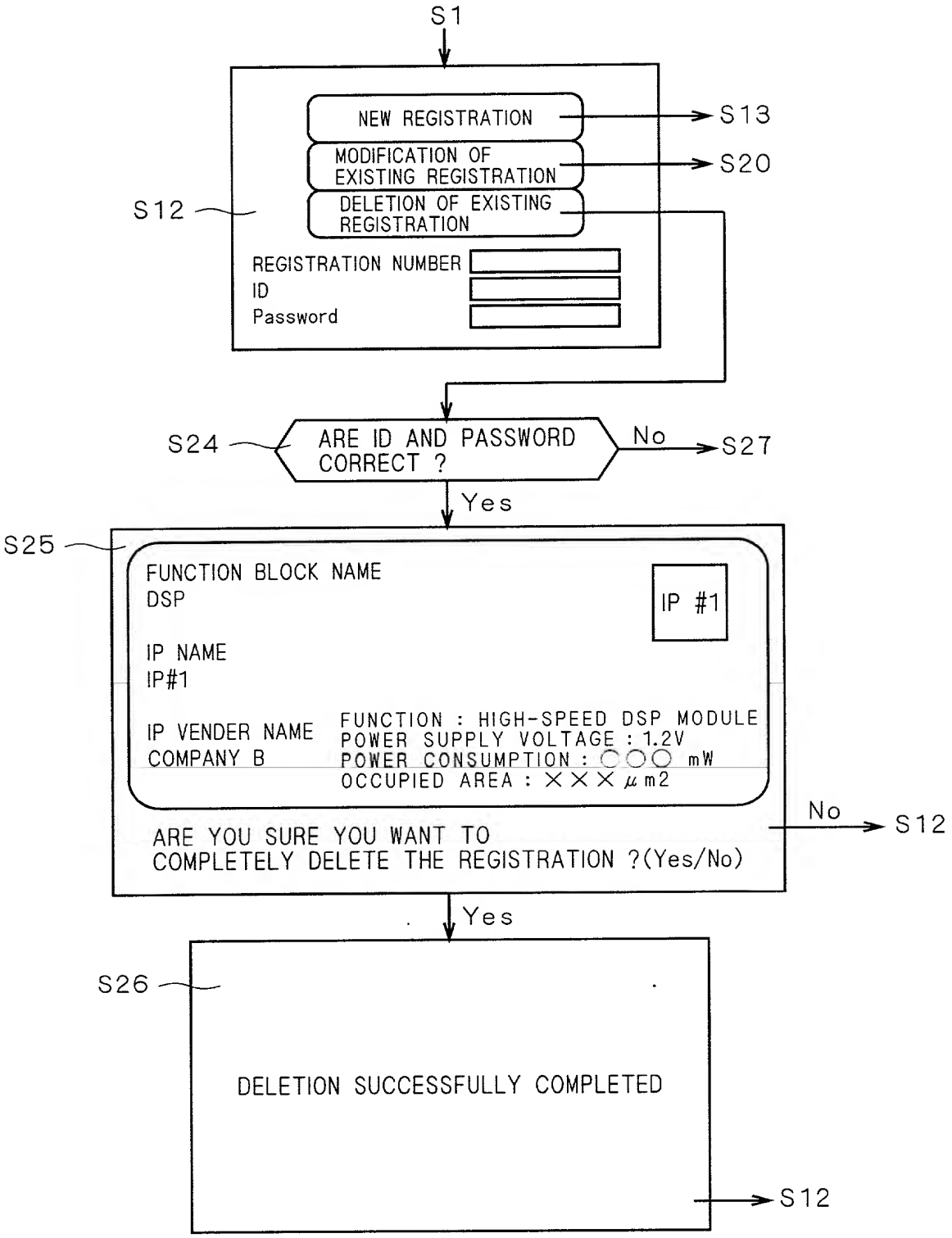

S1
NEW REGISTRATION
S13
MODIFICATION OF EXISTING REGISTRATION
S20
S12
DELETION OF EXISTING REGISTRATION
REGISTRATION NUMBER
ID
Password
S24
ARE ID AND PASSWORD CORRECT ?
No
S27
Yes
S25
FUNCTION BLOCK NAME
DSP
IP #1
IP NAME
IP#1
IP VENDER NAME
COMPANY B
FUNCTION : HIGH-SPEED DSP MODULE
POWER SUPPLY VOLTAGE : 1.2V
POWER CONSUMPTION : ○○○ mW
OCCUPIED AREA : ×××μm2
ARE YOU SURE YOU WANT TO COMPLETELY DELETE THE REGISTRATION ?(Yes/No)
No
S12
Yes
S26
DELETION SUCCESSFULLY COMPLETED
S12

FIG. 20

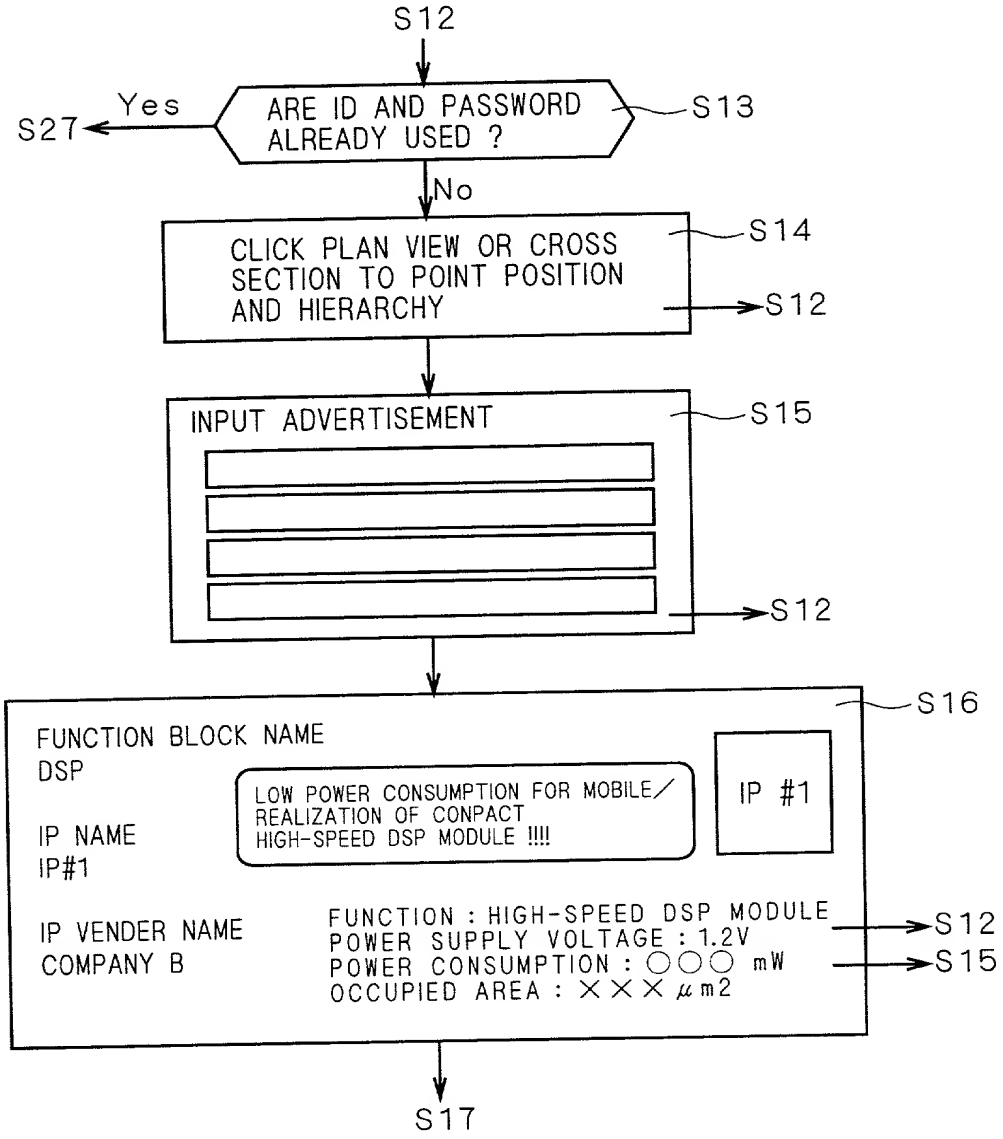

S12
Yes
S27
ARE ID AND PASSWORD ALREADY USED ?
S13
No
CLICK PLAN VIEW OR CROSS SECTION TO POINT POSITION AND HIERARCHY
S14
S12
INPUT ADVERTISEMENT
S15
S12
S16
FUNCTION BLOCK NAME
DSP
LOW POWER CONSUMPTION FOR MOBILE/ REALIZATION OF CONPACT HIGH-SPEED DSP MODULE !!!!
IP #1
IP NAME
IP#1
IP VENDER NAME
COMPANY B
FUNCTION : HIGH-SPEED DSP MODULE
POWER SUPPLY VOLTAGE : 1.2V
POWER CONSUMPTION : ○○○ mW
OCCUPIED AREA : ××× μm2
S12
S15
S17

FIG. 21

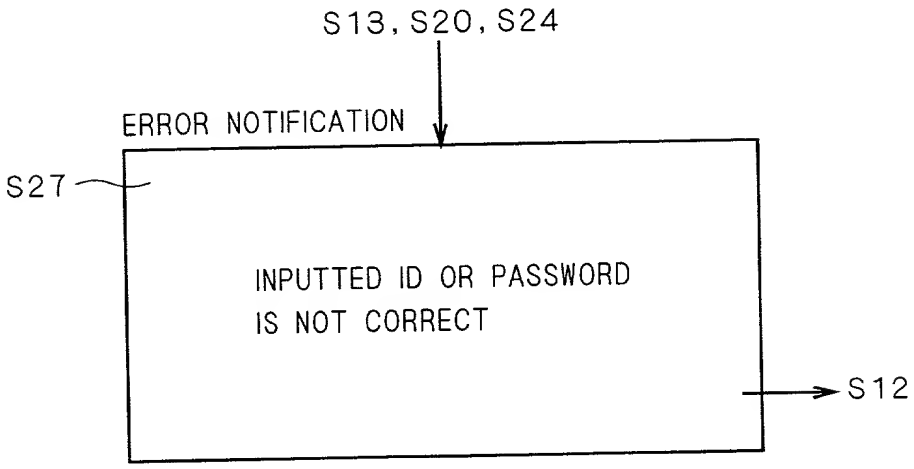

S13, S20, S24
ERROR NOTIFICATION
S27
INPUTTED ID OR PASSWORD
IS NOT CORRECT
S12

FIG. 22

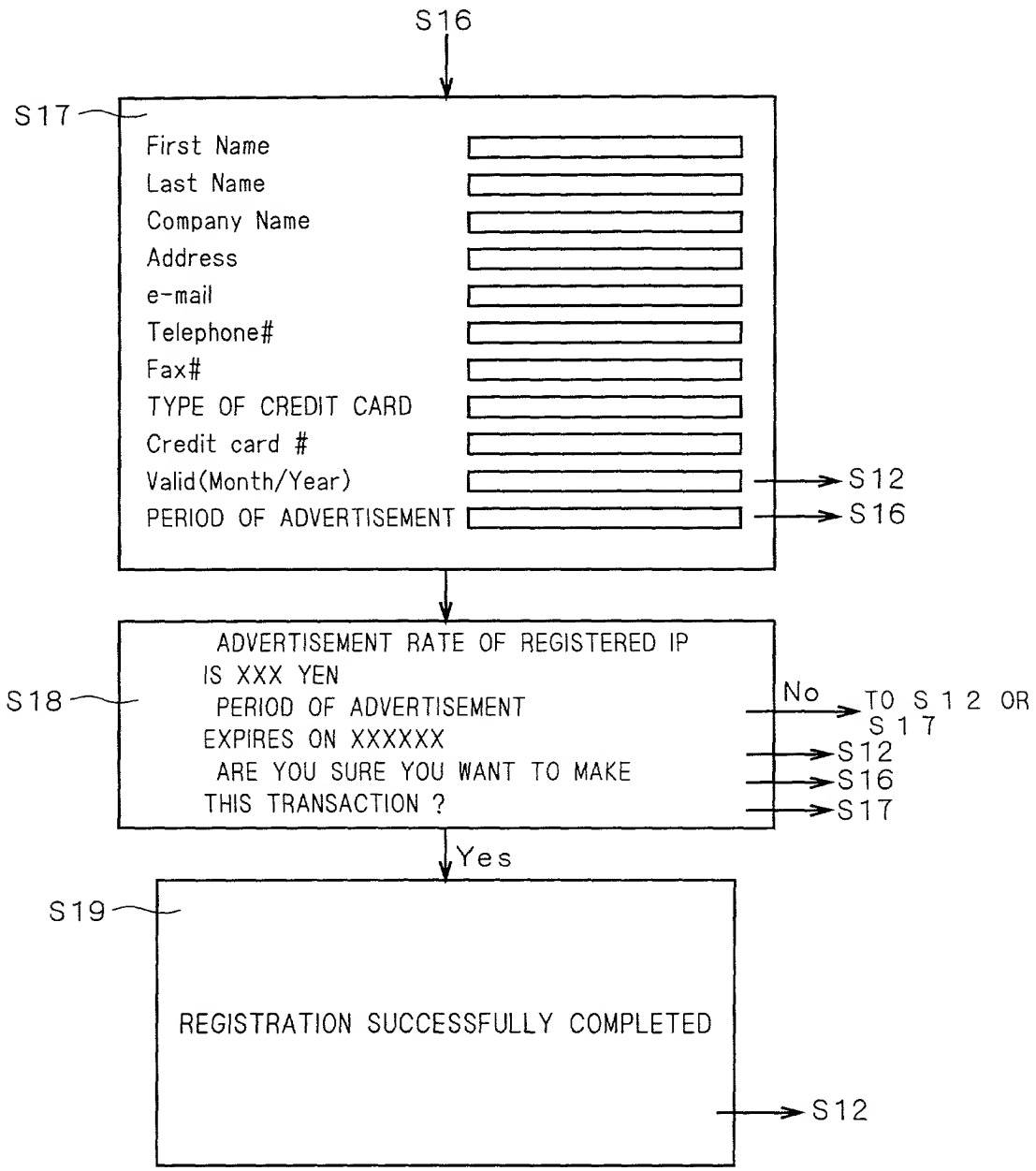

S16
S17
First Name
Last Name
Company Name
Address
e-mail
Telephone#
Fax#
TYPE OF CREDIT CARD
Credit card #
Valid(Month/Year)
PERIOD OF ADVERTISEMENT
S12
S16
S18
ADVERTISEMENT RATE OF REGISTERED IP IS XXX YEN
PERIOD OF ADVERTISEMENT EXPIRES ON XXXXXX
ARE YOU SURE YOU WANT TO MAKE THIS TRANSACTION ?
No
TO S12 OR S17
S12
S16
S17
Yes
S19
REGISTRATION SUCCESSFULLY COMPLETED
S12

FIG. 23

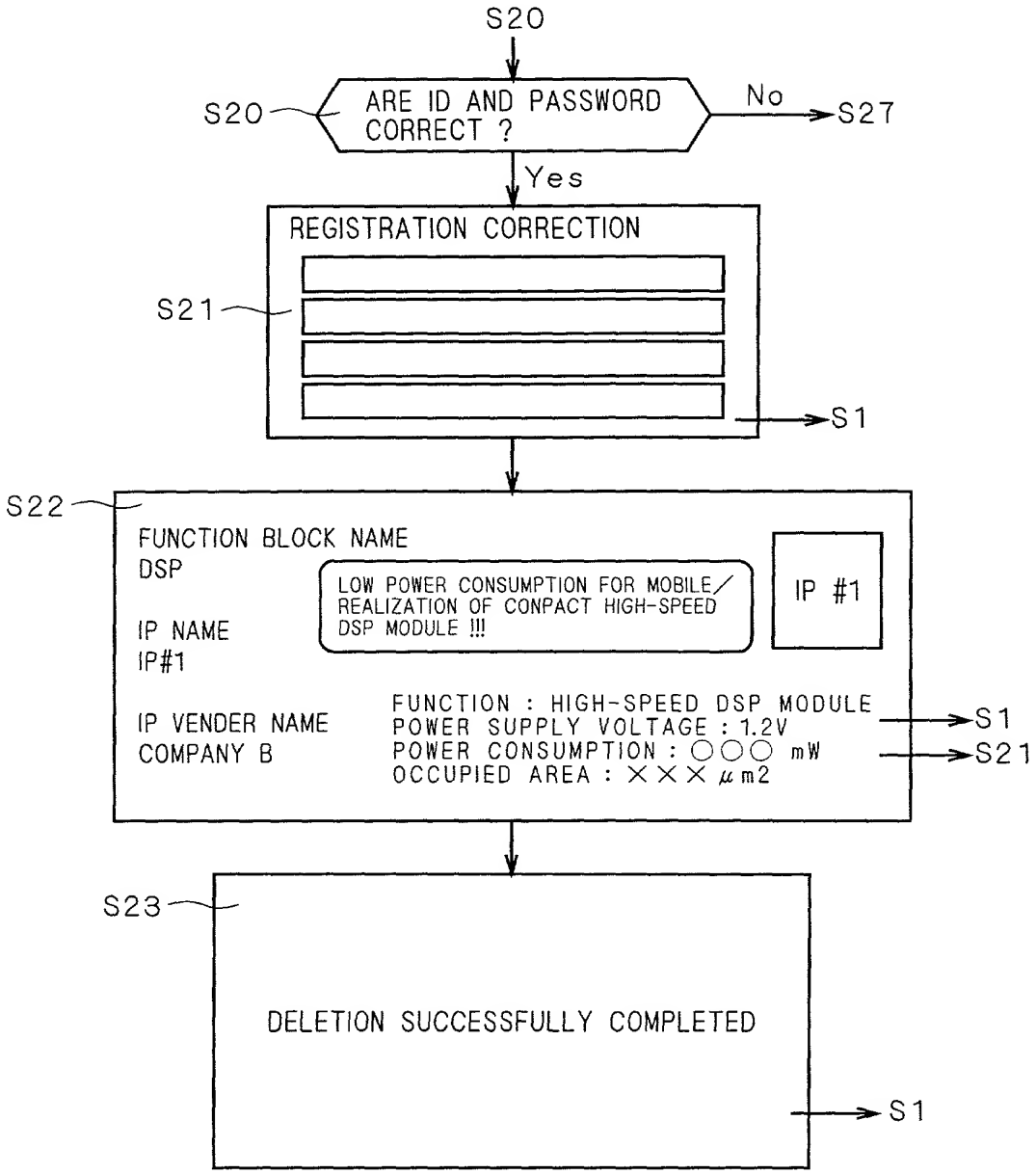

S20
S20
ARE ID AND PASSWORD CORRECT ?
No
S27
Yes
REGISTRATION CORRECTION
S21
S1
S22
FUNCTION BLOCK NAME
DSP
LOW POWER CONSUMPTION FOR MOBILE/ REALIZATION OF CONPACT HIGH-SPEED DSP MODULE !!!
IP #1
IP NAME
IP#1
IP VENDER NAME
COMPANY B
FUNCTION : HIGH-SPEED DSP MODULE
POWER SUPPLY VOLTAGE : 1.2V
POWER CONSUMPTION : ○○○ mW
OCCUPIED AREA : ××× μm2
S1
S21
S23
DELETION SUCCESSFULLY COMPLETED
S1

FIG. 24

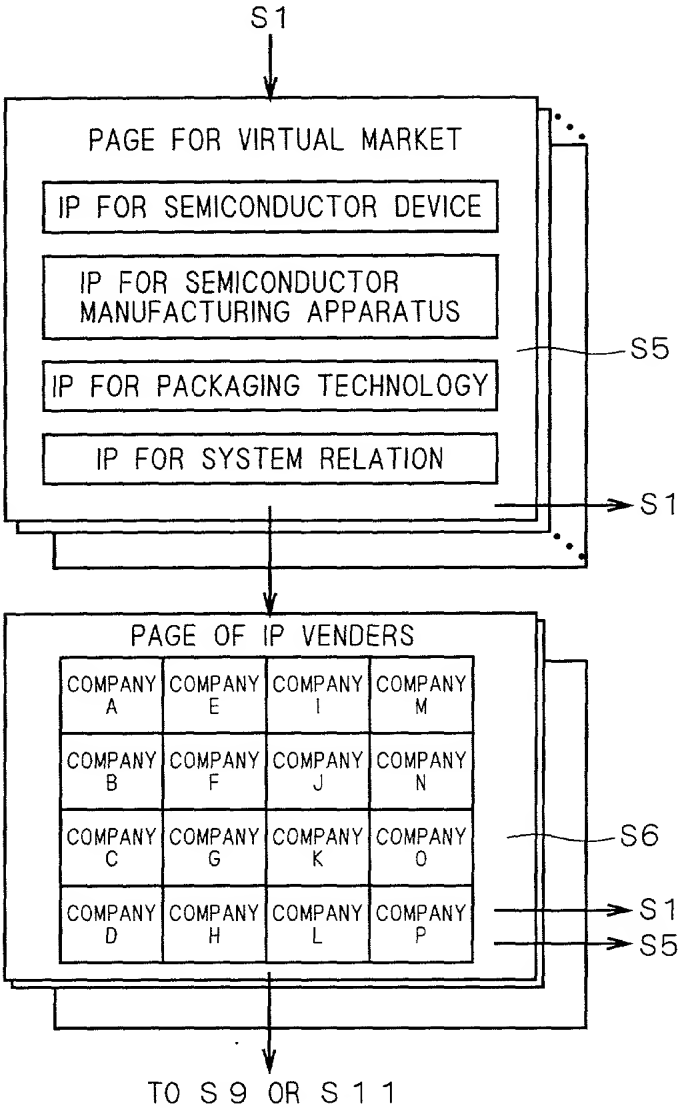

S1
PAGE FOR VIRTUAL MARKET
IP FOR SEMICONDUCTOR DEVICE
IP FOR SEMICONDUCTOR MANUFACTURING APPARATUS
IP FOR PACKAGING TECHNOLOGY
IP FOR SYSTEM RELATION
S5
S1
PAGE OF IP VENDERS
COMPANY A
COMPANY E
COMPANY I
COMPANY M
COMPANY B
COMPANY F
COMPANY J
COMPANY N
COMPANY C
COMPANY G
COMPANY K
COMPANY O
COMPANY D
COMPANY H
COMPANY L
COMPANY P
S6
S1
S5
TO S9 OR S11

FIG. 25

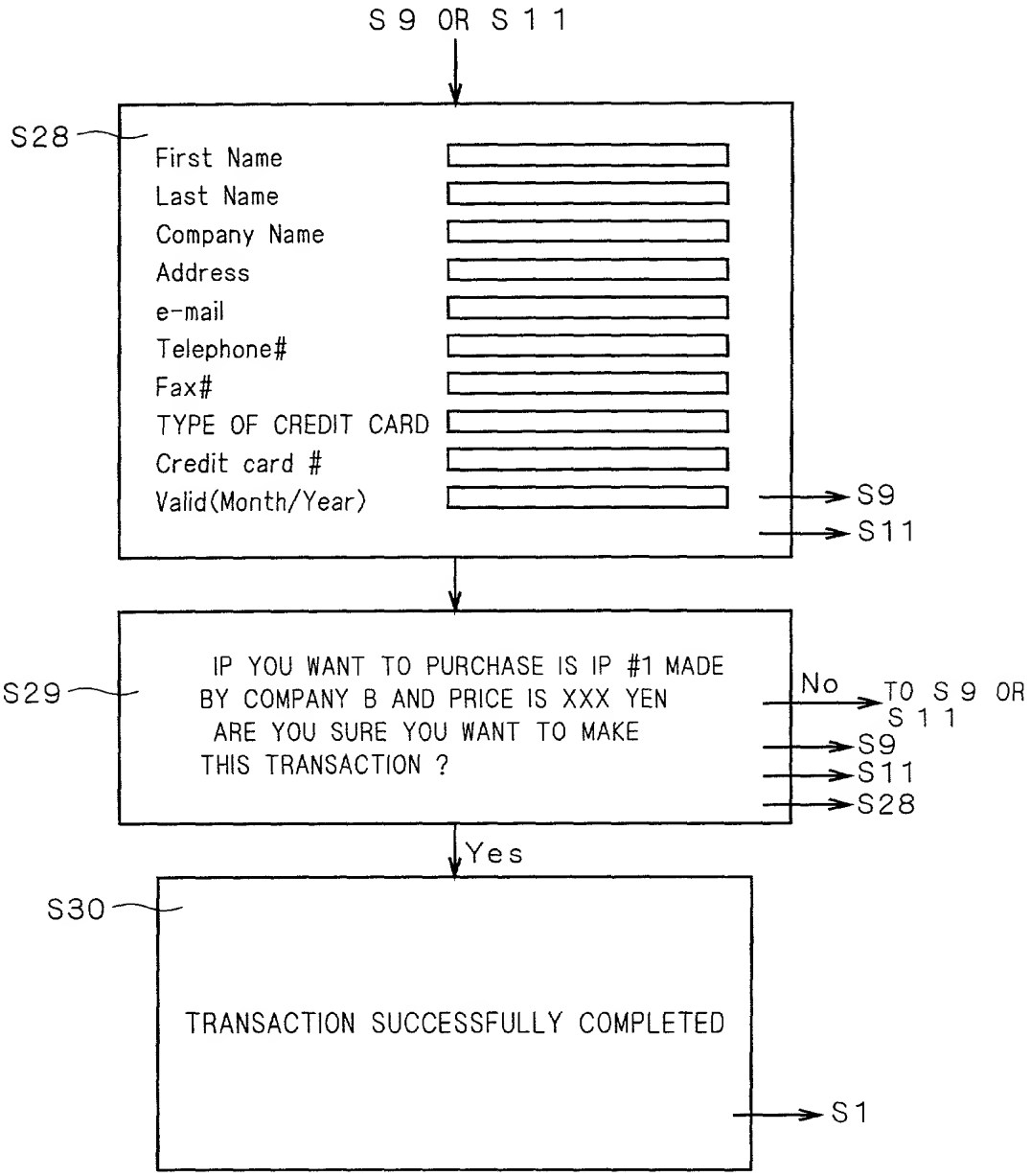

S9 OR S11
S28
First Name
Last Name
Company Name
Address
e-mail
Telephone#
Fax#
TYPE OF CREDIT CARD
Credit card #
Valid(Month/Year)
S9
S11
S29
IP YOU WANT TO PURCHASE IS IP #1 MADE BY COMPANY B AND PRICE IS XXX YEN ARE YOU SURE YOU WANT TO MAKE THIS TRANSACTION ?
No
TO S9 OR S11
S9
S11
S28
Yes
S30
TRANSACTION SUCCESSFULLY COMPLETED
S1

FIG. 26

P10

SPECIFICATION LIST OF IP #001

1. MEMORY MACROCELL(SRAM)

- ●HIGH-SPEED MEMORY(1port) MAXIMUM 256Kbit CYCLE TIME 1GHz
- ●HIGH-SPEED MEMORY(2port) MAXIMUM 512Kbit CYCLE TIME 700MHz

2. CORE LINEUP

●COMMUNICATION	ATM(Asynchronous Transfer Mode)
●GRAPHICS	DRAC(Direct Rambus Asic Cell),NTSC/PAL ENCODER
●MOBILE	DSP(Digital Signal Processing)
●COMPUTER AND HOME ELECTRONICS	MPEG4 ENCODER/DECODER
●HIGH-SPEED INTERFACE	AGP(Accelerated Graphics Port)